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<u>L6</u>	(module or DIMM or SIMM or card) near8 (data near4 bus)	1940	<u>L6</u>

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99%

 J. D. Nicoud , K. Skala

ACM SIGARCH Computer Architecture News , Proceedings of the 13th annual international symposium on Computer architecture June 1986

Volume 14 Issue 2

In order to build lower cost multimicroprocessor systems, a narrow synchronous bus (15 active lines) is proposed. It multiplexes address and data on 8 bits, and arbitrates in two pipe-lined cycles on four lines. Due to the 20 to 40 MHz bus clock, and the pipelined control logic, the performances are equivalent to Multibus-2, IEEE-P896 and similar 32-bit buses. For the implementation, cards are disposed radially around a special connector. The very short co ...

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